

REMARKS

Claims 1-6 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

INFORMATION DISCLOSURE STATEMENT

The Examiner alleges that the information disclosure statement (IDS) filed May 4, 2004 fails to comply with 37 CFR 1.98(a)(1). Applicant thanks the Examiner for the thorough examination of the IDS. Applicant notes that the omission of the cited co-pending applications in a Form PTO-1449 is intentional to avoid printing of the applications on any subsequently issued patents, and hence, becoming publicly available.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-5 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tsang et al. (U.S. Pat. No. 5,900,623). This rejection is respectfully traversed.

With respect to claim 1, Tsang fails to show, teach, or suggest that the circuit for changing a gate-applied voltage applies at least one of a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in an accumulation state, and another predetermined voltage from a second voltage source to the gates of the plurality of transistors while in a reading out state. Instead, Tsang appears to disclose that gates of the alleged transistors are always connected to the same source.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. Scripps Clinic & Res. Found. V. Genentech, Inc., 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. Constant v. Advanced Micro-Devices, Inc., 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Tsang fails to disclose the limitation of applying another predetermined voltage from a second voltage source to the gates of the plurality of the transistors while in a reading out state.

As shown in an exemplary embodiment in FIG. 2 of the present application, first and second voltage sources that are each coupled to the circuit for changing the gate-applied voltage. The circuit applies a first voltage from the first voltage source to gates of each of a plurality of transistors, and applies a second voltage from the second voltage source. In other words, during different periods, multiple voltage sources are applied to the same gates. More specifically, the first voltage source is applied to multiple gates during a first state and the second voltage source is applied to the same multiple gates during the second state.

As shown in FIG. 4 of Tsang, each transistor N1-N5 appears to always be connected to the same source during the accumulation state and the reading out state. In other words, N1 is always connected to SCB, and N2 is always connected to SC. In particular, none of the transistors are connected to different sources specifically during the two different states as claim 1 recites.

REJECTION UNDER 35 U.S.C. § 103

Claims 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsang et al. (U.S. Pat. No. 5,900,623). This rejection is respectfully traversed.

With respect to claim 6, Tsang fails to disclose that the circuit for changing gate-applied voltage selectively applies the first and second voltage outputs based on an accumulation enable signal and a reading out enable signal, respectively.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, Tsang fails to disclose the limitation that the circuit selectively applies the first and second voltage outputs based on an accumulation enable signal and a reading out enable signal, respectively.

As shown in an exemplary embodiment in FIG. 2 of the present application, a voltage supply circuit VCLi generates a gate voltage VPGi and a drain voltage VPDi. As described in Paragraphs [0055] and [0070], the voltage supply circuit VCLi receives an accumulation enabling signal SDI and a reading-out enabling signal SDR2. The voltage supply circuit VCLi generates the gate voltage based on which of the enabling signals SDI and SDR2 is asserted.

In contrast, Tsang appears to be absent of any teaching or suggestion of this structure. For example, the Examiner relies on FIG. 4 of Tsang to teach voltage supplies SCB and SC to transistors N1 and N2, respectively. Applicants respectfully

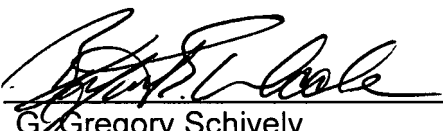
note that neither FIG. 4 nor any other figure of Tsang appears to disclose an accumulation enable signal and a reading out enable signal. Applicants respectfully submit that claim 6 should be allowable for at least the above reason.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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By: 
Gregory Schively
Reg. No. 27,382

Bryant E. Wade
Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

GGs/BEW/dms